Abstract

A test pattern generation and comparison circuit creates test pattern stimulus signals for and evaluates response signals from logic or memory such as random access memory (RAM). It utilizes both parallel and serial interfaces to the logic/memory under test. The test pattern generation and comparison circuit further provides a method for testing logic and memory utilizing built-in self test (BIST) techniques. The method uses a programmable logic/memory commands which are translated into physical logic signals and timings for the logic or memory under test. The results of the test pattern generated and applied to the logic or memory are compared to expected results. The result of the comparison is a pass/fail designation. In addition, the comparison of the expected test results with the actual test results provides information on the exact location of the failure. Also, since the test pattern generation and comparison circuit architecture is compatible with hardware description languages such as Verilog HDL or VHDL, the test pattern generation and comparison circuit can be automatically generated with a silicon compiler.